coupled to the first selected Y-line exceeds a respective threshold level of current, and for generating the first read signal accordingly;

said integrated circuit further comprising an output circuit coupled to receive at least the first read signal, for generating an output signal derived from at least the first read signal.

A1 cont.

REMARKS

In response to the Examiner's Restriction Requirement, the undersigned provisionally elects Group I, being claims 1-39 and 50-54, with traverse. Withdrawal of the Restriction Requirement is respectfully requested.

Claim 40 (from Group II) has been re-written to depend from independent claim 29 (from Group I). In particular, amended claim 40 now limits the second mode of operation introduced in claim 29 to a test mode of operation.

The recitation of the first selected Y-line near the end of the claim provides unambiguous antecedent support, and is now consistent with the claim as originally presented.

Applicant respectfully submits the restriction is improper, and requests the withdrawal of the restriction requirement, thereby proceeding with the examination of claims 1-68.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Andrew C. Graham — 2/24/03 Date

Respectfully submitted,

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APPENDIX A

MARKED-UP VERSION OF CLAIM TO SHOW CHANGES:

40. (Amended) ~~An integrated circuit comprising:~~ The integrated circuit defined by claim 29 wherein:

each memory cell comprises a passive element memory cell including an anti-fuse;

the X-line circuit comprises a first X-line circuit;

the first mode of operation comprises a read mode of operation;

the second mode of operation comprises a test mode of operation;

~~a fully-decoded array of passive element memory cells, each memory cell comprising an anti-fuse and coupled to one of a plurality of X-lines and one of a plurality of Y-lines, wherein each Y-line is associated with a plurality of X-lines by virtue of the memory cells respectively coupled therebetween;~~

~~a first X-line circuit for selecting, in a read mode of operation, an X-line associated with a first selected Y-line to impress a read bias across a corresponding memory cell coupled between the selected X-line and the first selected Y-line, and for selecting, in a test mode of operation, a first plurality of X-lines associated with the first selected Y-line to impress the read bias across each of a corresponding first plurality of selected memory cells respectively coupled between the first plurality of selected X-lines and the first selected Y-line;~~

the ~~a~~ first read circuit is for determining, in both the read and test modes of operation, whether an aggregate read current of the one or more selected memory cells coupled to the first selected Y-line exceeds a respective threshold level of current, and for generating the ~~a~~ first read signal accordingly;

said integrated circuit further comprising an output circuit coupled to receive at least the first read signal, for generating an output signal derived from at least the first read signal.